

**AMENDMENTS TO THE CLAIMS**

The following listing of claims replaces all prior versions and listings of claims in the application.

1. (Currently Amended) A conductive line for a semiconductor device including:
  - a first conductive layer;
  - a Titanium layer; and
  - a first Titanium rich Titanium Nitride layer between the first conductive layer and the Titanium layer; and
  - a second Titanium rich Titanium Nitride layer, and wherein the first conductive layer is between the first and second Titanium rich Titanium Nitride layers.
2. (Original) A conductive line according to claim 1, wherein the first conductive layer is in direct contact with the first Titanium rich Titanium Nitride layer.
3. (Previously Presented) A conductive line according to claim 1, wherein the Titanium layer is in direct contact with the first Titanium rich Titanium Nitride layer.
4. (Previously Presented) A conductive line according to claim 1, wherein the first conductive layer is a metal layer.
5. (Original) A conductive line according to claim 4, wherein the first conductive layer is an aluminium alloy.
6. (Original) A conductive line according to claim 5, wherein the aluminium alloy is an aluminium copper alloy.
7. (Previously Presented) A conductive line according to claim 1, wherein the Titanium layer is less than about  $500 \times 10^{-10}$ m (500 Angstroms) thick.

8. (Original) A conductive line according to claim 7, wherein the Titanium layer is from about 60 -  $110 \times 10^{-10}$ m (60 - 110 Angstroms) thick.
9. (Previously Presented) A conductive line according to claim 1, wherein the first Titanium rich Titanium Nitride layer is a  $250 - 500 \times 10^{-10}$ m (250 - 500 Angstroms) layer.
10. (Previously Presented) A conductive line according to claim 1, wherein the first conductive layer is a  $4000 - 8000 \times 10^{-10}$ m (4000 - 8000 Angstroms) layer.
11. (Cancelled)
12. (Currently Amended) A process for manufacturing a conductive line, comprising the steps of:
  - depositing a Titanium layer onto a substrate;
  - depositing a first Titanium rich Titanium Nitride layer to the other side of said Titanium layer relative to said substrate; and
  - depositing a first conductive layer to the other side of said first Titanium rich Titanium Nitride layer relative to said Titanium layer; and
  - depositing a second Titanium rich Titanium Nitride layer to the other side of said first conductive layer relative to said first Titanium rich Titanium Nitride layer.
13. (Original) A process according to claim 12, wherein the Titanium layer is deposited directly onto said substrate.
14. (Previously Presented) A process according to claim 13, wherein the first Titanium rich Titanium Nitride layer is deposited directly onto said Titanium layer.
15. (Previously Presented) A process according to claim 13, wherein the first conductive layer is deposited directly onto said first Titanium rich Titanium Nitride layer.

16. (Cancelled)
17. (Previously Presented) A process according to claim 12, wherein the first conductive layer is a metal layer.
18. (Original) A process according to claim 17, wherein the first conductive layer is an aluminium alloy.
19. (Original) A process according to claim 18, wherein the aluminium alloy is an aluminium copper alloy.
20. (Previously Presented) A process according to claim 12, wherein the Titanium layer is less than about 500 x 10-10m (500 Angstroms) thick.
21. (Original) A process according to claim 20, wherein the Titanium layer is from about 60 - 110 x 10-10m (60 - 110 Angstroms) thick.
22. (Previously Presented) A process according to claim 12, wherein the first Titanium rich Titanium Nitride layer is a 250 - 500 x 10-10m (250 - 500 Angstroms) layer.
23. (Previously Presented) A process according to claim 12, wherein the first conductive layer is a 4000 - 8000 x 10-10m (4000 - 8000 Angstroms) layer.
24. (Previously Presented) A silicon substrate having a plurality of conductive lines according to claim 1 thereon.
25. (Previously Presented) A semiconductor device including one or more conductive lines according to claim 1.

26. (Previously Presented) A memory including one or more conductive lines according to claim 1.

27. (Previously Presented) An integrated circuit including one or more conductive lines according to claim 1.